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 Chao Wang, Frank Mueller, Christian Engelmann, Stephen L. Scott
 November 2008 SC '08: Proceedings of the 2008 ACM/IEEE conference on
 Publisher: IEEE Press
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As the number of nodes in high-performance computing environments k
 faults are becoming common place. Reactive fault tolerance (FT) often c
 due to massive I/O requirements and relies on manual job resubmission

- 2 [Proactive fault tolerance for HPC with Xen virtualization](#)
 Arun Babu Nagarajan, Frank Mueller, Christian Engelmann, Stephen L. Sco
 June 2007 ICS '07: Proceedings of the 21st annual international conference
 Supercomputing
 Publisher: ACM
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Large-scale parallel computing is relying increasingly on clusters with th
 processors. At such large counts of compute nodes, faults are becoming
 Current techniques to tolerate faults focus on reactive schemes to recov

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 Ronny Krashinsky, Christopher Batten, Krste Asanović
 July 2008 Transactions on Design Automation of Electronic Systems
 Volume 13 Issue 3
 Publisher: ACM
 Full text available: ☒ Pdf (11.74 MB) Additional Information: [full citation](#), [abstract](#), [reference](#)
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The Scale vector-thread processor is a complexity-effective solution for
 computing which flexibly supports both vector and highly multithreaded
 7.1-million transistor chip has 16 decoupled execution clusters, vector k

Keyw ords: Vector processors, hybrid C++/Verilog simulation, iterative


flow, multithreaded processors, procedural datapath pre-placement, vector processors

- 4 [High-performance ethernet-based communications for future multi-core](#)
 Michael Schiassner, Nagabhushan Chittur, Erwin Oertli, Paul M. Stillwell, Jr, Dennis Bradford, Richard J. Carter, Jayaram Mudigonda, Nathan Binkert, N November 2007 SC '07: Proceedings of the 2007 ACM/IEEE conference on Supercomputing
 Publisher: ACM

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Data centers and HPC clusters often incorporate specialized networking system requirements. However, Ethernet's low cost and high performance shift from specialized fabrics toward standard Ethernet. Although Ethernet

- 5 [FaCSim: a fast and cycle-accurate architecture simulator for embedded systems](#)
 Jaemin Lee, Junghyun Kim, Choonki Jang, Seungkyun Kim, Bernhard Egger, SangYong Han
 June 2008 LCTES '08: Proceedings of the 2008 ACM SIGPLAN-SIGBED conference on Languages, compilers, and tools for embedded systems
 Publisher: ACM

Full text available:  Pdf (664.75 KB) Additional Information: [full citation](#), [abstract](#), [references](#)

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There have been strong demands for a fast and cycle-accurate virtual platform in the embedded systems area where developers can do meaningful software development including performance debugging in the context of the entire platform.

Keywords: architecture simulator, cycle-accurate simulation, full-system simulator parallelization, virtual prototyping

Also published in:

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